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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/525,999	11/28/2005	Stefan Horeth	12951-7	6219

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EXAMINER	
PARIHAR, SUCHIN	

ART UNIT	PAPER NUMBER
2825	

MAIL DATE	DELIVERY MODE
09/04/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/525,999	HORETH ET AL.	
	Examiner	Art Unit	
	SUCHIN PARIHAR	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 June 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7 and 9-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7 and 9-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 June 2008* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This NON-FINAL office action is in response to application 10/525,999, amendment filed on 6/11/2009. Claims 1-7 and 9-17 are currently pending in this application.

2. Applicant's arguments filed 6/11/2009 have been fully considered. Upon further consideration, a new ground(s) of rejection is made.

Drawings

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the elements/features of claim 1 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New

Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

4 The specification is objected to because it fails to identify appropriate sections and fails to distinguish features of the invention from features of the prior art. Correction is required.

The following guidelines illustrate the preferred layout for the specification of a utility application. These guidelines are suggested for the applicant's use.

Arrangement of the Specification

As provided in 37 CFR 1.77(b), the specification of a utility application should include the following sections in order. Each of the lettered items should appear in upper case, without underlining or bold type, as a section heading. If no text follows the section heading, the phrase "Not Applicable" should follow the section heading:

(a) TITLE OF THE INVENTION.
(b) CROSS-REFERENCE TO RELATED APPLICATIONS.
(c) STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT.
(d) THE NAMES OF THE PARTIES TO A JOINT RESEARCH AGREEMENT.
(e) INCORPORATION-BY-REFERENCE OF MATERIAL SUBMITTED ON A COMPACT DISC.
(f) BACKGROUND OF THE INVENTION.
    (1) Field of the Invention.
    (2) Description of Related Art including information disclosed under 37 CFR 1.97 and 1.98.
(g) BRIEF SUMMARY OF THE INVENTION.
(h) BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING(S).
(i) DETAILED DESCRIPTION OF THE INVENTION.
(j) CLAIM OR CLAIMS (commencing on a separate sheet).
(k) ABSTRACT OF THE DISCLOSURE (commencing on a separate sheet).
(l) SEQUENCE LISTING (See MPEP § 2424 and 37 CFR 1.821-1.825. A "Sequence Listing" is required on paper if the application discloses a

nucleotide or amino acid sequence as defined in 37 CFR 1.821(a) and if the required "Sequence Listing" is not submitted as an electronic document on compact disc).

Claim Rejections - 35 USC § 101

5 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

6 **Claims 1-7 and 9-13 are rejected under 35 U.S.C. 101** because the claimed invention is directed to non-statutory subject matter.

7. Claims 1–7 and 9-13 are non-statutory because a § 101 process claim must (1) be tied to another statutory class (a particular machine or apparatus) or (2) transform underlying subject matter (such as an article or materials) to a different state or thing; see In Re Bilski, 545 F.3d 943, 88 USPQZd 1385 (Fed. Cir. 2008). If neither of these requirements are met by the claim, the method is not a patent eligible process under § 101.

A § 101 process claim that would not qualify as a statutory process would be a claim that recites purely mental step(s) that can be performed manually or merely manipulating an abstract idea without the use of a specific structure. Thus, to qualify as a § 101 statutory process, the claimed step(s) must explicitly recite the other statutory class such as machine (i.e., the computer, the thing) to which it is tied, for example by identifying the machine/computer that accomplishes the step(s) and providing transformation underlying subject matter to a different state or thing to provide meaningful, reasonable limits and a practical application.

Claim 1 recites a series of process steps, but the steps neither explicitly recite a specific machine/computer that implements the claimed steps nor identify transformation of underlying subject matter to a different state or thing.

Thus, the subject matter of claim 1 is non-statutory and not patent eligible.

Claims 2-7 and 9-13 are rejected because they depend directly or indirectly from claim 1.

In order to comply with the 35 USC § 101 statutory requirement, a limitation, i.e., "by using a computer" must be inserted in one of the claimed steps of claim 1. This would be a tie and would overcome the 35 USC § 101 non-statutory issue, as long as the subject matter of the computer implementing the step is supported by the disclosure.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. **Claims 1, 4-6, 9-12 and 14-17 are rejected under 35 U.S.C. 103(a)** as being unpatentable over Jain et al. (US 6,301,687) in view of Jain et al. (US 6,484,292).

10. With respect to claims 1, 14 and 16-17, Jain ('687) teaches:

(a) determining (determining, i.e. verifying, Col 1, lines 45-60) for at least one specific circuit structure (circuit structure, see Abstract) described by the reference description (design specification, Col 1, lines 45-55) of the digital circuit (digital circuit

designs, see Abstract), wherein for the at least one specific circuit structure (circuit structure, see Abstract) a plurality of different implementation alternatives (different implementations of the same design, Col 1, lines 45-55) are known, in each case that an implementation alternative that has the greatest degree of structural equivalence (checking equivalence by verifying the using different implementations, Col 1, lines 45-55) with the digital circuit to be verified (original specification, Col 1, lines 45-55), is determined, whereby the different implementation alternatives are simulated respectively (pattern simulations used to determine functionally equivalent patterns or nodes, Col 6, lines 25-50), using random pattern simulation (see Jain, '687, Figure 2A, 108) and compared (different implementations of the same design are compared to the circuit design, Col 1, lines 45-55) with a corresponding simulation of the digital circuit (extensive simulation to produce the "golden specification", Col 1, lines 30-55), in order to determine as the implementation alternative with the greatest degree of structural equivalence (checking equivalence by verifying using different implementations, Col 1, lines 45-55) with the digital circuit, the implementation alternative, which in this case for several simulation patterns (first implementation .... it becomes the specification for the next implementation comparison, Col 1, lines 50-65) has the greatest equivalence of design points (pattern simulations used to determine functionally equivalent patterns or nodes, Col 6, lines 25-50) with the digital circuit,

(b) replacing (it becomes [i.e. replaces] the specification for the next implementation, Col 1, lines 45-60) in the reference description of the digital circuit, the description of the individual circuit structures is replaced (once the implementation is

verified successfully, it becomes the specification for the next implementation comparison, Col 1, lines 45-55) by the implementation alternative determined for the respective circuit structure in step (a) with the greatest degree of structural equivalence (different implementations of the same design are compared to check their equivalence, Col 1, lines 45-60, results in the implementation with the greatest degree of equivalence being chosen or pointed out) in each case, and

(c) executing (verification executed, Col 3, lines 15-25) the equivalence test is executed by comparing the digital circuit with the reference description changed in accordance with step (b) (the next change in the specification is then compared to determine equivalence with the next implementation, Col 1, lines 45-55).

Jain ('687) fails to teach:

a plurality of different pre-defined implementation alternatives.

However, Jain ('292) teaches:

a plurality of different pre-defined (prior circuit implementations, see Abstract) implementation alternatives (see Figure 4, initial implementation and new design netlist, i..e several different pre-defined implementations that are read).

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate Jain ('292') into the invention of Jain ('687) for at least the following reason: Jain ('292) improves the invention of Jain ('687) by providing a method that enables a design to only re-implement parts of the design that have changed from a previous design cycle (see Jain '292, Col 1, lines 30-50).

11. With respect to claim 15, Jain ('687) teaches:

wherein a digital circuit to be verified (first implementation to be verified, Col 1, lines 45-60) is compared with a reference description (original specification [i.e. reference description], Col 1, lines 45-60) of the digital circuit, in order, to recognize errors (to catch design errors early in the design cycle, Col 1, lines 45-50) in the digital circuit using an equivalence test (verifying the equivalence of two boolean networks, Col 2, lines 10-20), the method comprising:

(a) determining (determining, i.e. verifying, Col 1, lines 45-60) for specific circuit structures (circuit structure, see Abstract) described by the reference description (design specification, Col 1, lines 45-55) of the digital circuit (digital circuit designs, see Abstract), for which different implementation alternatives (different implementations of the same design, Col 1, lines 45-55) are known, in each case that an implementation alternative that has the greatest degree of structural equivalence (checking equivalence by verifying the using different implementations, Col 1, lines 45-55) with the digital circuit to be verified (original specification, Col 1, lines 45-55), is determined, whereby the different implementation alternatives are simulated respectively (pattern simulations used to determine functionally equivalent patterns or nodes, Col 6, lines 25-50) in combination with the reference description and compared (different implementations of the same design are compared to the circuit design, Col 1, lines 45-55) with a corresponding simulation of the digital circuit (extensive simulation to produce the "golden specification", Col 1, lines 30-55), in order to determine as the implementation alternative with the greatest degree of structural equivalence (checking equivalence by verifying using different implementations, Col 1, lines 45-55) with the digital circuit, the

implementation alternative, which in this case for several simulation patterns (first implementation .... it becomes the specification for the next implementation comparison, Col 1, lines 50-65) has the greatest equivalence of design points (pattern simulations used to determine functionally equivalent patterns or nodes, Col 6, lines 25-50) with the digital circuit,

(b) replacing (it becomes [i.e. replaces] the specification for the next implementation, Col 1, lines 45-60) in the reference description of the digital circuit, the description of the individual circuit structures is replaced (once the implementation is verified successfully, it becomes the specification for the next implementation comparison, Col 1, lines 45-55) by the implementation alternative determined for the respective circuit structure in step (a) with the greatest degree of structural equivalence (different implementations of the same design are compared to check their equivalence, Col 1, lines 45-60, results in the implementation with the greatest degree of equivalence being chosen or pointed out) in each case, and

(c) executing (verification executed, Col 3, lines 15-25) the equivalence test is executed by comparing the digital circuit with the reference description changed in accordance with step (b) (the next change in the specification is then compared to determine equivalence with the next implementation, Col 1, lines 45-55).

Jain ('687) fails to teach:

a plurality of different pre-defined implementation alternatives.

However, Jain ('292) teaches:

a plurality of different pre-defined (prior circuit implementations, see Abstract) implementation alternatives (see Figure 4, initial implementation and new design netlist, i.e several different pre-defined implementations that are read).

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate Jain ('292') into the invention of Jain ('687) for at least the following reason: Jain ('292) improves the invention of Jain ('687) by providing a method that enables a design to only re-implement parts of the design that have changed from a previous design cycle (see Jain '292, Col 1, lines 30-50).

12. With respect to claim 4, Jain ('687) teaches:

wherein the process is executed computer-aided (computer-aided design, see Col 1, lines 10-15).

13. With respect to claim 5, Jain ('687) teaches:

wherein the reference description is selected from the group comprising RTL, VHDL and verilog descriptions (the original design is represented as an RTL design, Col 1, lines 45-55).

14. With respect to claim 6, Jain ('687) teaches:

the equivalence test is executed by comparing the digital circuit with the reference description changed in accordance with step (b) (the next change in the specification is then compared to determine equivalence with the next implementation, Col 1, lines 45-55).

15. With respect to claim 9, Jain ('687) teaches:

wherein for each circuit structure, the different implementation alternatives are simulated at the same time and compared with the simulation of the digital circuit (extensive simulation and comparing different implementations of the same design to check for equivalence, i.e. verification, Col 1, lines 45-55).

16. With respect to claim 10, Jain ('687) teaches:

wherein the different implementation alternatives for each circuit structure are simulated at the same time by inputs (test vectors that represent all possible inputs to the system, Col 1, lines 1-30) of the implementation alternatives being connected with one another and corresponding outputs (outputs of these test vectors are analyzed, Col 1, lines 1-30) of the implementation alternatives being led to a common output (common output, see Figure 13A) to maintain the circuit function of the individual implementation alternatives.

17. With respect to claim 11, Jain ('687) teaches:

wherein the outputs of different implementation alternatives are connected by a logic OR link to the common output (see Figure 13A).

18. With respect to claim 12, Jain ('687) teaches:

wherein for each implementation alternative in step (a). the degree of equivalence with the simulation of the digital circuit is obtained by the number of the values output for the individual simulation patterns of the reference description with the respective implementation alternative, the alternative values identically output, which are identical to the values output by the digital circuit for the corresponding simulation patterns, being determined for the several simulation patterns for each implementation

alternative and being used as degree of equivalence for the corresponding implementation alternative (outputs are analyzed to try to verify their equivalence, Col 14, lines 40-45).

19. **Claims 2, 3 and 7 are rejected under 35 U.S.C. 103(a)** as being unpatentable over Jain et al. (US 6,301,687) in view of Jain et al. (US 6,484,292) and in further view of Higgins et al. (6,993,730).

20. With respect to claim 2, Jain ('687) in view of Jain ('292) fails to teach:

wherein the specific circuit structures for which the implementation alternative with the greatest degree of equivalence is determined in each case, are multiplier structures.

However, Higgins teaches:

wherein the specific circuit structures for which the implementation alternative with the greatest degree of equivalence is determined in each case, are multiplier structures (equivalencies between two multiplier circuits, Col 12, lines 25-35).

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate Higgins into the invention of Jain ('687) and Jain ('292) for at least the following reason: Higgins improves the invention of Jain/Jain combination by providing a method that can determine equivalence between two circuit models much quicker than previously attainable in the prior art (see Abstract, Higgins).

21. With respect to claim 3, Higgins teaches:

wherein he specific circuit structures, for which the implementation alternative with the greatest degree of equivalence is determined in each case, are multiplier

structures for realizing integral multiplication function (equivalencies between two multiplier circuits, Col 12, lines 25-35).

22. With respect to claim 7, Jain ('687) in view of Jain ('292) fails to teach:

wherein the pre-defined implementation alternatives for the specific circuit structures comprise varying architectures of the specific circuit structures aided by a synthesis device available for the design of the digital circuit.

However, Higgins teaches more than one architecture for the specific circuit structures that are multipliers (equivalencies between two multiplier circuits, Col 12, lines 25-35).

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate Higgins into the invention of Jain ('687) and Jain ('292) for at least the following reason: Higgins improves the invention of Jain by providing a method that can determine equivalence between two circuit models much quicker than previously attainable in the prior art (see Abstract).

Response to Arguments

23. Applicant's arguments filed 6/11/2009 have been fully considered. Upon further consideration, a new ground(s) of rejection is made.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SUCHIN PARIHAR whose telephone number is (571)272-6210. The examiner can normally be reached on Mon-Fri, 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Paul Dinh/
Primary Examiner, Art Unit 2825

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Examiner, Art Unit 2825